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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/762,111

01/21/2004

Thomas Teuschler

WSAG 0144 PUS

3905

22045

7590

10/12/2006

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EXAMINER

NGUYEN, TUAN H

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

38

Office Action Summary

Application No.

10/762,111

Applicant(s)

TEUSCHLER ET AL.

Examiner

Tuan H. Nguyen

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 4-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-3, 5-9 in the reply filed on 10/17/05 is acknowledged. The traversal is on the ground(s) that "the surface flatness near the edge of the wafer cannot be accomplished by a materially different process such as lapping or grinding", and "Applicant are unaware of any method of grinding overlapping in the prior art which is capable of addressing departures from planarity in the edge region". This is not found persuasive because attached are references that show processes for producing the claimed polished semiconductor wafer by lapping or grinding without the step of wet etching. (See Kato et al., process I in fig. 1 and the result in fig. 7; or Moriya et al., process in fig. 1 and result in fig. 4).

The requirement is still deemed proper and is therefore made FINAL.

Applicant's election with traverse of Species I, claims 1-3 in the reply filed on 7/14/06 is acknowledged. The traversal is on the ground(s) that "claim 1 is a generic claim". This is not found persuasive because Species I directs to a polished semiconductor wafer while species II draws to an arrangement for producing a polished semiconductor wafer including a shield. They are distinct species, and the semiconductor wafer of claim 1 is not a generic claim with respect to an arrangement in claim 5-9.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriya et al..

Moriya et al., fig. 4 and text in paragraph [0029] discloses the claimed polished semiconductor wafer having a maximum deviation of flatness of the back surface from an ideal plane in a range between R-6 mm and R-1 mm of the back surface is of 0.7 micron or less (see particular on page 2, right-hand col., first paragraph, “ both, of the major surfaces of the substrate 1 have a flatness of up to 0.5 micron and especially, up to 0.3 micron”.

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kato et al..

Kato et al., fig. 1, 7, and text in paragraphs [0064]-[0068] that shows the polished semiconductor wafer using process I, having the whole back surface flatness of less than 0.7 micron that includes the claimed range between R-6 mm and R-1 mm as claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(e) as being unpatentable over Kato et al. in view of Wenski et al. (cited ref.).

Kato et al., figs. 1, 7 and text in paragraph [0064]-[0068] discloses the claimed polished semiconductor wafer having back surface flatness of less than 0.7 micron as explained above, except the front surface is formed by an epitaxially deposited layer.

Wenski et al., in a related art, teaches on col. 3, last paragraph, the polished wafer could be an epitaxially deposited layer.

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It would have been obvious to one having ordinary skill in the art at the time the invention was made to polished the wafer composed of a homogeneous material or the production of layered semiconductor substrates such as epitaxial layer since they are well-known material for used as a substrate in semiconductor art.


Response to Arguments

Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Tuan H. Nguyen
Primary Examiner
Art Unit 2813